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Structural evaluation of sol–gel derived lead strontium titanate diffusion barrier for integration in lead zirconate titanate transducer design

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ABSTRACT

Sol–gel derived $Pb_{40}Sr_{60}TiO_3$ (PST) thin film has been investigated as a diffusion barrier for integrating in $PbZr_{30}Ti_{70}O_3$ (PZT) device structures on Si substrates. PST film was deposited on SiO_2/Si substrate and annealed at a relatively low temperature range of 550–600 °C producing a crack-free, smooth and textured surface. Following deposition on PST/SiO_2/Si template PZT thin film was crystallised exhibiting random grain orientations and an insertion of the bottom Pt/Ti electrode forming PZT/Pt/Ti/PST/SiO_2/Si stacks promoted the preferred PZT (111) perovskite phase. PZT (111) peak intensity gradually decreased along with slight increase of the PZT (110) peak with increasing annealing temperature of the buffer PST film. The dielectric and ferroelectric properties of the PZT with barrier PST deposited at 550 °C were assessed. The dielectric constant and loss factor were estimated as 390 and 0.034 at 100 kHz respectively and the remnant polarisation was 28 μC/cm^2 at 19 V. The performance of the PZT/PST device structures was compared to similar PZT transducer stacks having widely used barrier TiO_2 layer.

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1. Introduction

The nucleation, growth and perovskite phase transformation of lead zirconate titanate, $PbZr_xTi_{(1-x)}O_3$ (PZT) thin films have been extensively investigated in recent years due to its potential for direct integration with well-established Si integrated circuit (IC) technology [1,2]. While a wide range of devices incorporating PZT thin film has been demonstrated, the major areas of applications are currently focussed on the prospects of micro-electromechanical system (MEMS) components and non-volatile memories [3,4]. Among various coating techniques developed to deposit PZT layers, chemical solution methods, for example sol–gel offer advantages such as easy composition control, homogeneity, relatively low process temperature and reduced manufacturing cost at wafer-scale production [5]. As MEMS device applications are concerned, a thin and mechanically stable structural layer is employed with PZT film deposited onto it and followed by further processing to realise on-chip sensing and actuation depending on specific device design. The most commonly used structural material is an active Si layer on SOI (silicon-on-insulator) wafers. Another choice is silicon nitride, Si_3N_4 (SiN_x) layer, as it can be prepared with low stress on standard Si substrates and is cost-effective compared to SOI wafers. Ideally, the PZT device structures consist of PZT thin film sandwiched between two electrodes and usually integrated onto a Si substrate, typically resembling a planar capacitor layer design. The quality of PZT thin film and its fatigue behaviour depend on various factors such as thermal compatibility of the compositional layers, interfaces, the microstructures, crystal defects and oxygen vacancies, thereby influencing the performance and reliability of the PZT microdevices [2,6]. Other challenges in integrating ferroelectric films for MEMS device applications include the suppression of interdiffusion of the constituent elements, control of the compositional fluctuation in multilayer stacks and thermal stress [5,7].

It is now established in PZT transducer design that thermal stability of the electrodes is crucial for high quality deposition of the PZT thin film, and platinum (Pt) is widely used as a bottom electrode because of its stability and good lattice match to PZT film [5,6]. In addition, Pt provides the fleeting formation of favourable intermetallic phase, Pt_3Pb promoting nucleation and the formation of preferred PZT (111) perovskite phase during crystallisation of PZT films [5,7]. However, a suitable diffusion barrier layer must be inserted between the bottom Pt/Ti electrode and Si substrate to limit the diffusion of lead (Pb) during PZT crystallisation at elevated temperature in an oxidising atmosphere, thereby preventing microcracks and delamination caused by Pt hillock formation [8]. The buffer layer plays a significant role in improving interfaces in PZT device structures and could provide better adhesion between the substrate and PZT device layer enabling favourable PZT microstructure formation having homogeneous grain distribution [2,9]. The structural evaluation of the diffusion barrier is necessary to understand its influence on phase nucleation during PZT crystallisation, in optimisation of the PZT transducer stack designs and enhancement of the piezoelectric

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performance. Until recently most research studies have been considered with incorporating various types of oxides and intermetallic materials as the diffusion barrier to obtain crack-free PZT film on its top. Barrier layers studied extensively include TiO_2, ZrO_2, Al_2O_3, Ti–Al, Ir(Pt)/TiN and $LaNiO_3$, produced using a range of deposition techniques [7,9,10]. In this paper, we have presented a simple and inexpensive alternative by incorporating sol–gel derived lead strontium titanate, $Pb_{(1-x)}Sr_xTiO_3$, (PST) thin film as barrier scheme and investigated the microstructural and electrical properties of the PZT/PST stacks, focussing on improvement in PZT device properties. Furthermore, the recent quest in the microelectronics industry to replace native SiO_2 with high dielectric constant (high-k) oxides for miniaturisation has established that an atomically abrupt interface between Si and strontium titanate is, in fact, achievable under controlled process conditions producing a Sr-passivated substrate resembling H-terminated (hydrogen) Si surface [11]. The result is of great significance in interfacing high-k materials with Si and unfolds greater prospects in engineering $(Ba,Sr)TiO_3$:$PbTiO_3$ solid solution systems to fabricate electronic and optical devices in direct integration on Si chip [12]. In particular, PST system shows only one phase transition compared to three transitions in $Ba_xSr_{1-x}TiO_3$ solid solutions [12] and has additional benefits from the relatively low processing temperature and a linear variation of the Curie temperature with Sr^{2+} content [12,13]. In addition, the PST film has similar perovskite-type crystal structure and lattice mismatch of only ~3% to PZT film [12], making it a potential candidate to insert in PZT transducer design as a diffusion barrier. In integrating PZT microdevices at wafer-scale, it is often desirable to deposit PZT thin film on non-uniform surface by modifying the process layout that allows patterning of the bottom Pt/Ti electrode as the first step, prior to spin-coating of the PZT. This is primarily because patterning of the PZT transducer stacks by plasma etching starting from top electrode to bottom substrate sequentially may introduce damage to the device layers and degrade ferroelectric properties of the functional PZT material. However, there is possibility in the modified process design with initial patterning of the bottom electrode that PZT may suffer from post-annealing issues such as PZT bubbling and microcracks during PZT crystallisation on a patterned $Pt/Ti/SiO_2/Si$ substrate without a barrier layer. A crack-free PST layer as a diffusion buffer could prevent such PZT blistering on a patterned $Pt/Ti/PST/SiO_2/Si$ stacks and is expected to be beneficial to wafer-scale integration of the PZT microdevices. Moreover, high quality PST film can be deposited cheaper with easy composition control using the sol–gel method, similar to PZT film deposition, thus reducing the process complexity, undesired damage to PZT device layer and overall process time. In this work, we propose an alternative and suitable scheme to realise PZT device structures incorporating PST as a diffusion barrier layer for future prospects of MEMS device integration. The surface morphology, film orientations and electrical properties of the PZT/PST stacks on Si substrates were evaluated.

2. Experiments

2.1. Fabrication — PZT/PST thin film stacks

While pursuing investigation on suitability of the PST thin film as a diffusion barrier, the trials were conducted primarily on standard SiO_2/Si substrates. In addition, a further effort had been made to study the PST film deposited on Si_3N_4 (SiN_x) structural layer having a thickness of 1500 nm that was grown by low-pressure chemical vapour deposition (LPCVD) on Si substrates and low stressed. In preparation of various types of PZT and PST thin films a sol gel method was employed. The detail of the PZT sol preparation was reported previously in the literature [5,14]. The composition of PZT solution was chosen as Zr/Ti = 30/70 and the concentration of the resulting solution was 0.4 M based on Pb content. Initially PST film was synthesised as described in Section 2.1.1, before a Pt/Ti bottom electrode was deposited onto the $PST/SiO_2/Si$ template by sputtering technique. A thin seed layer of Ti (8 nm) was first deposited by RF sputtering to act as an adhesion promoter between the buffer PST film and Pt electrode. Following this, Pt with a 100 nm thickness was deposited using DC sputtering without breaking vacuum. PZT thin films were finally deposited by spin-coating the solution at 3000 rpm for 30 s onto barrier layer stacks, e.g., $PST/SiO_2/Si$ depending on trials conditions under consideration. Following spin-coating PZT thin film stacks underwent pyrolysis and crystallisation hotplate bakes at 200 °C for 45 s and 530 °C for 5 min in air respectively. The final thickness of around 550 nm was selected for PZT thin film in these experiments unless stated otherwise.

2.1.1. PST deposition

In our present study $Pb_{40}Sr_{60}TiO_3$ ($PS_{60}T$) thin film having Pb/Sr = 40/60 compositions was chosen as a diffusion barrier. Fig. 1 shows a schematic process flow of sol gel route to prepare the (Pb,Sr)(Ti,Mn)O_3 precursor solution and the film deposition process using a modified version of the route as reported in the literature [15]. It should be noted that Mn-doping is not always necessary to prepare a $PS_{60}T$ film to insert as a barrier layer in PZT device structures. Sr content is the most important in PST solid solution systems to form a stable diffusion barrier because Sr atoms first occupy the trough between Si–O dimer rows, thus preventing the diffusion of Pb into the Si [11]. In this case, Mn-doping was chosen as 1%. As can be seen the precursor solution was derived from soft chemical processing of various solvents and complex reagents. Lead acetate and strontium acetate were dissolved in a stoichiometric ratio in a 5:8 mixture of 1.3-propanediol and acetic acid. Stirring along with slightly heating above room temperature ensured to obtain a clear solution. Meanwhile, 3.245 g of titanium butoxide and 0.0495 g of manganese acetate were mixed in a glove box and diluted in 15 ml acetic acid. Both solutions were mixed together and stirred at room temperature overnight around 16 h. The next stage was to dilute the solution with 2-methoxyethanol up to a volume of 50 ml to obtain the desired concentration of the resulting solution to 0.4 M that gave rise to the final PST sol prior to spin-coating on the substrates for specific design and device structures. The wafer coated with PST layer was further baked on a hotplate at 350 °C for 10 min to evaporate the solvents before

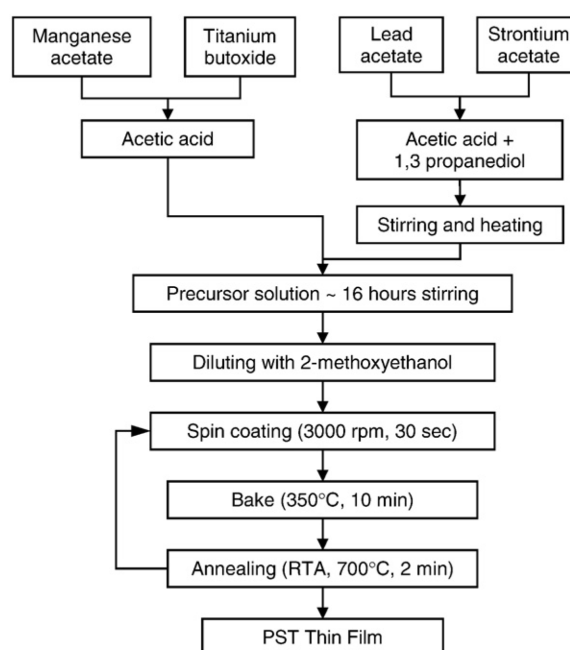

Fig. 1. Schematic process flow of the PST thin film deposition by a sol–gel technique.

underwent final crystallisation stage on a hotplate at elevated temperature ranging from 550 °C to 700 °C for 15 min or annealed in a RTA (rapid thermal annealer) for 2 min in compressed air depending on trials procedure and requirements. The single layer coating at 3000 rpm for 30 s produced a PST layer thickness of around 40 nm and the process can be repeated to obtain thicker films.

2.2. Sample preparation and measurements

Series of samples coated with PST thin film under different deposition conditions were prepared to conduct trials with the aim of optimising quality and thickness of the buffer PST layer. PST films were spin-coated on SiO_2/Si substrates and annealed at different temperatures of 550 °C, 600 °C, 650 °C and 700 °C to evaluate their microstructural properties. In one of such trials, an attempt had been made to deposit PST layer on bare Si by etching away the top thermal oxide, i.e. SiO_2 layer using buffered HF. A few samples were also prepared with buffer PST deposited on SiN_x structural layer at similar range of crystallisation temperatures as mentioned above. Following initial investigation of the PST/SiO_2/Si composites, deposition trials were extended to study the microstructures and film orientations of the PZT transducer stacks by depositing PZT film on buffer PST surface. In this case, PZT film was spin-coated onto diffusion barrier stacks of PST/SiO_2/Si without a bottom Pt/Ti electrode and also on platinised Si i.e., Pt/Ti/PST/SiO_2/Si structures. Furthermore, PZT film was deposited directly on SiO_2/Si and SiN_x/Si substrates to address the inherent problems of microcracks and PZT bubbling due to diffusion of Pb. The layer thicknesses chosen for buffer PST layer and PZT films were 40 nm and 550 nm respectively. In addition, a comparative study was performed by depositing titanium oxide (TiO_2) as a diffusion barrier to investigate the feasibility of the PST film as an alternative to commonly used barrier materials as proposed in this paper. The TiO_2 barrier of thickness 30 nm was prepared by RF sputtering of Ti followed by thermal oxidation at 700 °C using RTA that enabled the formation of stable rutile phase over the metastable anatase and brookite phases [16].

All the samples coated with PST and PZT films under different process conditions were characterised by X-ray diffraction (XRD) technique with CuK_α radiation at various intermediate stages of thin film deposition. The apparatus used was Siemens, D5005 diffractometer having Bragg–Brentano geometry. The surface morphology of PZT/PST composites was analysed using SEM (scanning electron microscopy) and AFM (atomic force microscopy) methods. FEI XL30-SFEG model was employed to obtain SEM images whereas DI Dimension 3000 was used for AFM analysis. AFM tip was of type of PPP-NCH-50, having length of 125 µm and resonant frequency of 204–497 kHz. In this study, AFM was operated in tapping mode. The electrical characterisation was carried out using Wayne Kerr 6425 precision component analyser to assess the dielectric properties of the PZT film having PST film underneath as a barrier. The capacitance measurements were conducted on PZT thin film capacitors by evaporating chrome/gold (Cr/Au) dots as top circular electrode of 0.8 mm diameter using a shadow mask. In addition, a ferroelectric test system having model RT66A from Radiant Technologies was utilised to perform polarisation hysteresis measurements on Cr/Au/PZT/Pt/Ti/PST/SiO_2/Si device structures. The ferroelectric behaviour of the PZT film under optimised deposition conditions of the buffer PST layer was evaluated consequently.

3. Results and discussions

3.1. Film orientation

The X-rays diffraction patterns of PST thin film deposited on SiO_2/Si substrates at different annealing temperatures of 550 °C, 600 °C, 650 °C and 700 °C are shown in Fig. 2. The XRD pattern of PST film on bare Si substrate crystallised at 650 °C was also analysed to study the possibility of replacing native SiO_2 with the PST in device design without degrading ferroelectric properties of the PZT film on its top. As can be seen from Fig. 2(a), PST annealed at 550 °C was randomly orientated due to its polycrystalline nature, and the (110) phase was also detected but the (110) peak was not sharp having very low intensity. This could be attributed to the early stage of crystallisation phase formation of PST film at lower annealing temperature of 550 °C and probably reflected the formation of mixed phases, e.g., interpenetrating nanocrystalline and amorphous phases. As the annealing temperature was further increased, the full crystallisation occurred revealing the fact that PST film was transformed into perovskite phases on both SiO_2/Si and bare Si substrates at and above 600 °C with no evidence of pyrochlore phase. The PST film exhibited a preferred (110) perovskite grain orientation and the lower peak intensity of (110) phase could be related to the thickness of the PST film, i.e., 1 coated layer of only ~40 nm considered in these trials. Fig. 3 shows the XRD patterns of the PST film on SiN_x/Si substrates annealed at temperatures of 550 °C and 650 °C that also confirmed the polycrystalline nature of the film with preferred (110) perovskite phase, resembling similar XRD patterns obtained from PST/SiO_2/Si composite. It was noticed that the (110) peak was more pronounced and sharper in PST/SiN_x/Si stacks compared to PST/SiO_2/Si stacks, for example the plots at 650 °C depicted in Fig. 3(b) and (c). The sharp and single-peak nature of PST (110) phase without any splitting indicate cubic or pseudo-cubic structure typically observed in $PS_{60}T$ thin films [17].

In order to study the growth and quality of the PZT on top of buffer PST layer the XRD analysis was carried out on a batch of samples

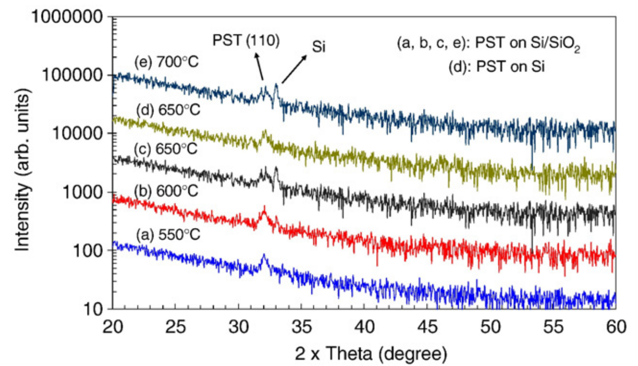

Fig. 2. XRD patterns of sol–gel deposited $Pb_{40}Sr_{60}TiO_3$ (PST) thin films on SiO_2/Si substrates and annealed at different temperatures (a) 550 °C, (b) 600 °C, (c) 650 °C and (e) 700 °C; (d) XRD pattern showing (110) peak of PST film on bare Si substrate (by etching away SiO_2 layer) annealed at 650 °C. PST film has thickness of 40 nm.

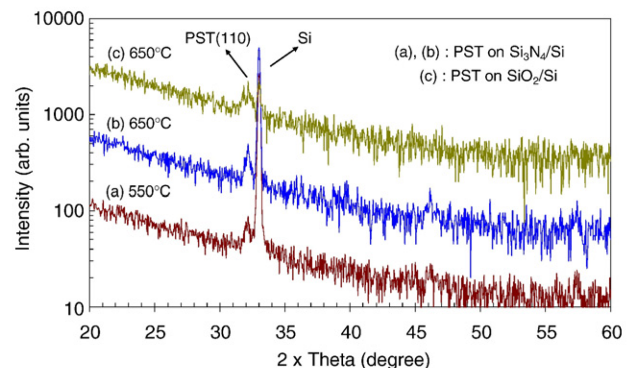

Fig. 3. XRD patterns of PST thin films deposited on Si_3N_4/Si substrates at different annealing temperatures (a) 550 °C and (b) 650 °C; (c) XRD pattern of PST on SiO_2/Si substrate deposited at 650 °C for comparison.

prepared with various types of device layer designs. These comprised of PZT deposited directly on $PST/SiO_2/Si$ stacks and on platinised Si substrates, for example $PZT/Pt/Ti/PST/SiO_2/Si$ stacks with buffer PST deposited at different annealing temperatures. As shown in Fig. 4, it was observed in all these device structures that the PZT film was preferentially (111) oriented having higher peak intensity and also exhibited a less preferred (110) orientation. The peak intensity of PZT (110) phase was lowest from the device structure with underlying PST annealed at 550 °C, and gradually became stronger with increasing crystallisation temperature of the PST. However, the PZT (111) peak has still higher intensity than (110) peak in all the samples revealing the fact that the piezoelectric properties in these device structures will be dominated by the preferred perovskite (111) grains as expected with PZT film of 30/70 compositions [5]. It was further noticed that the PZT device layer with buffer PST crystallised at 550 °C, as shown in Fig. 4(a), exhibited maximum intensity for preferred PZT (111) phase along with lowest intensity and broadest (110) peak compared to other samples having PST deposited at higher annealing temperatures. This could be attributed to the fact that the stronger PST (110) phase, caused by higher crystallisation temperature of the buffer PST layer, could produce nucleation sites enhancing unfavourable PZT (110) phase along with preferred (111) phase. We had investigated further the phase behaviour of PZT by estimating the relative intensity profile of dominant PZT (111) peak against annealing temperature of underlying PST layer with a focus on optimisation of PST crystallisation conditions. In one approach the relative intensity of PZT (111) peak was calculated by setting the intensity of the PZT (111) peak for the PZT/Pt/Ti/PST stacks with buffer PST deposited at 550 °C as unity and normalising other intensity profiles having PST crystallised at higher temperatures to this setting [18]. Secondly, we had estimated the relative intensity of PZT (111) peak by considering the influence of Pt (111) peak on the nucleation and growth of the PZT, e.g., $I_{rel} = I_{PZT}/(I_{Pt} + I_{PZT})$ where I_{PZT} and I_{Pt} were intensities of PZT (111) and Pt (111) respectively. The relative intensity profiles of PZT film illustrated in Fig. 5 exhibited similar nature of the plots for both types of evaluation methods. The results indicate strongest orientation of PZT preferred (111) phase when buffer PST layer annealed at 550 °C and a sharp decline in PZT (111) peak intensity at and beyond PST crystallisation temperature of 650 °C. The intensity of PZT (111) peak decreased by nearly 40% when annealing temperature of the underlying PST barrier increased from 550 °C to 650 °C. The initial XRD analysis revealed that annealing of PST diffusion barrier in the temperature range of 550–600 °C promotes PZT preferred (111) phase with a stronger peak and is, therefore, expected to produce high quality PZT device layer on its top in PZT transducer stacks.

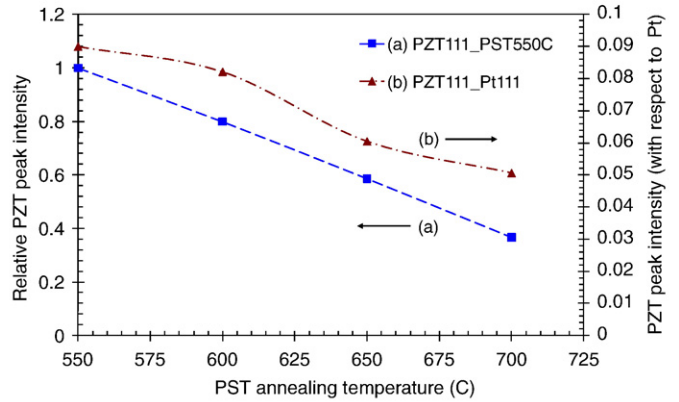

Fig. 5. Relative intensity profiles of PZT (111) peak as a function of annealing temperature of buffer PST layer in $PZT/Pt/Ti/PST/SiO_2/Si$ stacks (a) relative intensity calculated by setting the PZT peak intensity with PST deposited at 550 °C as unity; (b) estimated PZT peak intensity with respect to Pt (111) peak e.g. $I_{PZT}/(I_{Pt} + I_{PZT})$.

An experimental study was further undertaken to compare the performance of PST layer with other widely employed materials as a diffusion barrier. In this case TiO_2 was chosen as a buffer layer, as it was previously integrated to realise PZT FBAR devices (thin film bulk acoustic resonator) and FBAR filters for mobile phones [19]. In this study we had also selected the different combinations of structural layer and barrier, e.g. $PST/SiO_2/Si$ and $TiO_2/SiN_x/Si$ templates with PST and TiO_2 barrier deposited at 550 °C and 700 °C respectively. The comparative study is expected to give an insight to the crystallisation phase of the diffusion barrier and its influence on PZT microstructures and film orientations. Fig. 6(a) and (b) shows XRD patterns of PZT composites without a bottom Pt/Ti electrode, fabricated on both types of templates as mentioned above. XRD patterns of PZT on $PST/SiO_2/Si$ and $TiO_2/SiN_x/Si$ stacks exhibited similar polycrystalline nature of the PZT film having random orientations that comprised of (100), (110), (111), (200), (210) and (211) peaks and having low peak intensity. It was noted that the PZT (110) peak has slightly higher intensity compared to (100) and (111) peaks but broader, whereas PZT (111) peak was sharper. It is evident from XRD plots that the PZT stacks were not completely crystallised into perovskite structures to promote any preferred grain orientation in both cases. This is not quite surprising and reflects the need of a seed layer, in most cases a Pt seed layer with preferred (111) phase that enhances the PZT phase transformation introducing nucleation sites along with formation of intermetallic phase, Pt_3Pb and reducing the surface energy [5,20]. In fact, XRD

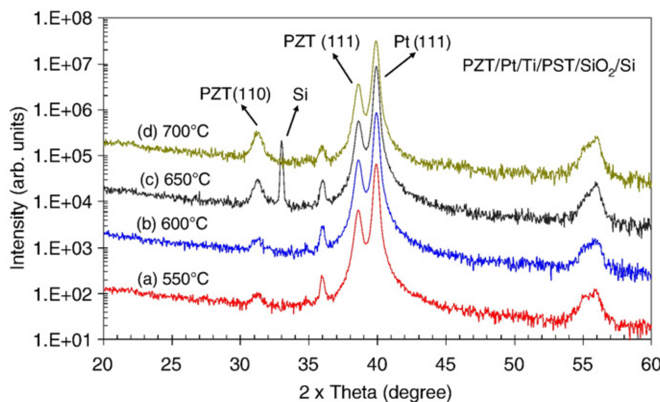

Fig. 4. XRD patterns of sol–gel deposited $PbZr_{30}Ti_{70}O_3$ (PZT) thin films on $Pt/Ti/PST/SiO_2/Si$ stacks with diffusion barrier PST layer deposited at different annealing temperatures (a) 550 °C, (b) 600 °C, (c) 650 °C and (d) 700 °C. PZT film has thickness of 550 nm.

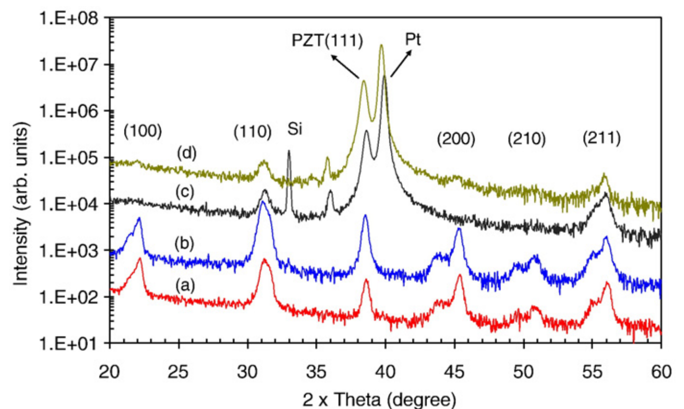

Fig. 6. Comparison of XRD patterns: (a) $PZT/PST/SiO_2/Si$ stacks with PST deposited at 550 °C, (b) $PZT/TiO_2/Si_3N_4/Si$ with TiO_2 deposited at 700 °C, (c) $PZT/Pt/Ti/PST/SiO_2/Si$ device structure and (d) $PZT/Pt/Ti/TiO_2/Si_3N_4/Si$.

analysis of the PZT device structures having Pt/Ti bottom electrode along with PST and TiO_2 barrier configurations as shown in Fig. 6(c) and (d) respectively exhibited a preferred (111) phase with higher peak intensity and a less preferred weaker (110) peak that established the well-crystalline PZT grain formation. It was further noticed that the PZT/Pt/Ti/TiO_2/SiN_x stacks showed also a diminished (100) peak and introduced a slight shift in Pt (111) and PZT (111) peaks towards lower angles in contrast to PZT/Pt/Ti/PST/SiO_2 structure. The relative shift in Pt and PZT peak positions reflected an incremental change in lattice parameters, when PZT films were deposited on different types of barrier and structural layers. XRD patterns of PZT deposited on Pt/Ti/PST/SiO_2 stacks look very similar to those obtained from the PZT device structures incorporating barrier TiO_2 layer, a commonly used material in PZT thin film devices and PZT-based MEMS components. Initial results established that the PST film was perfectly crystallised having preferred (110) perovskite phase on different types of structural layers and templates, e.g. SiO_2/Si and SiN_x/Si under carefully controlled process conditions and promoted PZT preferred (111) phase with stronger peak intensity in PZT transducer stacks as a diffusion barrier.

3.2. Microstructure evaluation

The surface morphology of the PST and PZT films on various types of templates was analysed using SEM and AFM methods to understand the impact of thermal annealing on the film texture. Fig. 7(a) and (b) shows the optical micrographs of the PZT surface as a clear evidence of the inherent problems of PZT bubbling and cracks that were observed during crystallisation step following spin-coating of the PZT on SiO_2/Si and SiN_x/Si substrates without an underlying electrode and diffusion barrier. The resulting surface was very poor showing discontinuities with formation of bubbles, pin-holes and microcracks that occurred due to diffusion of Pb from the sol into the SiO_2 or SiN_x layer during annealing and the formation of lead silicates causing delamination [1–5,18,19]. However, the PZT films often need to be deposited directly on SiO_2/Si and SiN_x/Si surface, in particular on patterned Pt/Ti bottom electrode configuration during wafer-scale integration of PZT thin film devices depending on specific process designs. To prevent the crazing effect and blistering of the overlying electrode, a suitable barrier layer is commonly incorporated in device structures prior to PZT coating [9,10,19]. Following deposition of buffer PST on SiO_2/Si substrates under different annealing conditions, the PST surface was found to be smooth and essentially no discontinuities in terms of crazing and microcracks as shown in Fig. 8. Fig. 8(a) exhibits SEM image of the PST layer on SiO_2/Si substrate at 550 °C under a low magnification scan, thereby exposing a large surface area that confirmed a crack-free texture of the PST film across the wafer, crucial for integration as a diffusion barrier in PZT transducer stacks. In this study the SEM scan was performed at an acceleration voltage of 10 kV. The surface of the PST film annealed at 550 °C appeared to be a random distribution of crystallite structures having spherical and circular shapes with a diameter of ~0.5–1.0 µm in a smooth matrix. The crystallites were not clustered to each other rather these crystallites resembled to isolated islands, probably reflecting the presence of interpenetrating nanocrystalline and amorphous phases [20]. Following scan with higher magnification shown in Fig. 8(b), the crystallite structure exhibited a fuzzy outer boundary having a diameter of ~100–150 nm and was embedded in a featureless and homogeneous matrix. It is evident from SEM analysis that the PST film crystallised at 550 °C gave rise to a random texture with essentially no preferred grain orientation as confirmed from XRD analysis depicted in Fig. 2(a). With increasing annealing temperature at and above 600 °C, the SEM analysis as shown in Fig. 8(c) and (d) revealed that the PST film had further developed into well-crystallised microstructures yielding dense and uniform grains. The larger grains were obtained at higher crystallisation temperature and however, PST film became more inhomogeneous. For example, PST film at 600 °C shown in Fig. 8(c) were composed of submicrometer-sized grains forming high density and closely-spaced islands that gave rise to a smooth and textured surface with rounded and uniform grain distribution. As the annealing temperature was further increased to 650 °C, more islands were formed and became distinguishable producing a dense microstructure composed of mostly perovskite (110) grains having larger size [21] but less uniform containing some porosity along the grain boundaries as illustrated in Fig. 8(d). In addition, the PST deposited on bare Si substrates without a native SiO_2 layer at 650 °C was evaluated as shown in Fig. 8(e). It is to be noted that SEM images shown in Fig. 8(d) and (e) were taken applying an acceleration voltage of 15 kV. PST film on bare Si produced a crack-free smooth surface that was developed into fine and uniform microstructures with flat crystal grains. This result looks very promising and indicates the formation of a good interface between the PST layer and Si substrate with future possibility of replacing native SiO_2 as proposed recently [11]. The average grain size in these films was estimated typically at about 100–150 nm as expected in $PS_{60}T$ film [12]. It is to be noted that PST microstructures also depend on Sr content and become denser having reduced grain size with the increase in Sr content [12,17].

In order to investigate the formation of interfaces including surface roughness of PST/SiO_2/Si and PZT/PST/SiO_2/Si stacks, AFM technique was employed. As shown in Fig. 9(a) and (b), the texture of buffer PST layer on SiO_2/Si substrates crystallised at 600 °C was denser and smoother compared to the PST surface annealed at higher temperature of 700 °C. The PST surface at 700 °C was essentially inhomogeneous with presence of small voids and porosity that are expected to

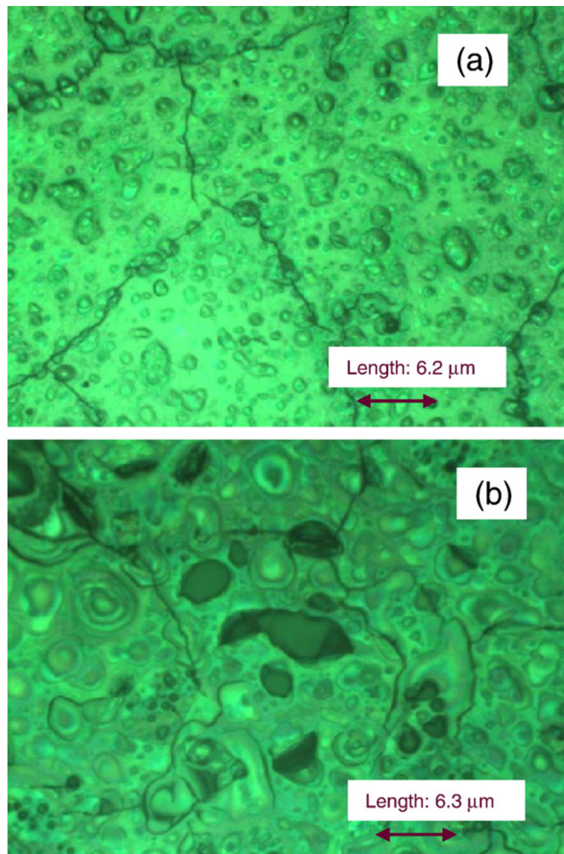

Fig. 7. Optical micrographs of the surface of PZT thin film deposited on structural layer show cracks and crazing effect (a) PZT/SiO_2/Si and (b) PZT/Si_3N_4/Si.

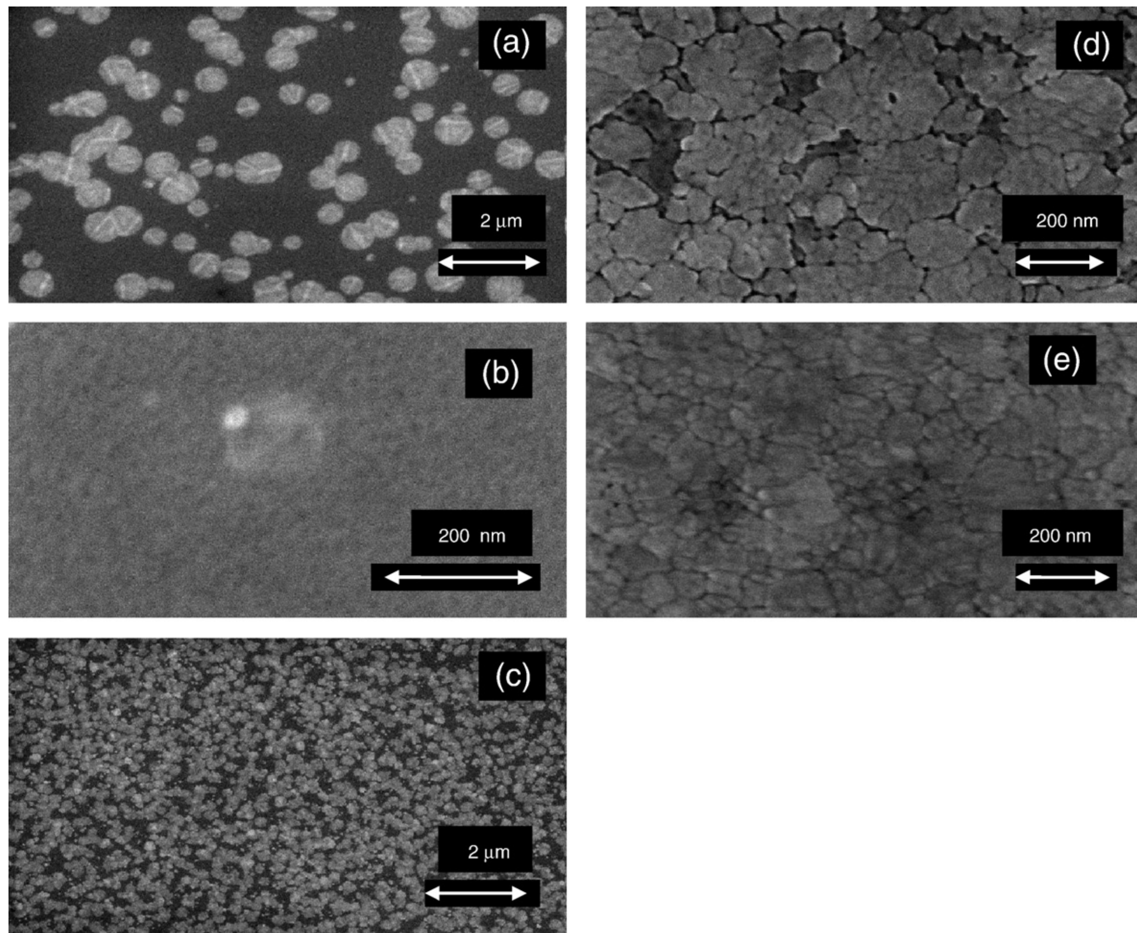

Fig. 8. SEM images of the PST film on SiO_2/Si substrates at different annealing temperature (a) PST/SiO_2/Si at 550 °C with a low magnification scan, (b) 550 °C with high magnification, (c) 600 °C, (d) 650 °C and (e) PST on bare Si (no SiO_2) at 650 °C.

introduce higher surface roughness and was confirmed by AFM surface analysis. The root mean square (RMS) values of surface roughnesses were estimated as 0.6 nm, 0.8 nm and 7.6 nm in PST/SiO_2/Si stacks crystallised at 550 °C, 600 °C and 700 °C respectively. The higher surface roughness of underlying PST film could degrade the quality of the PZT device layer that was reflected from XRD analysis of the PZT/PST composites with buffer PST deposited at 700 °C exhibiting lower intensity of PZT (111) peak depicted in Fig. 4. AFM surface morphology of PZT films on platinised Si substrates is illustrated in Fig. 10(a) and (b) respectively by considering two different types of templates, i.e. PZT/Pt/Ti/PST/SiO_2/Si structure with buffer PST deposited at 550 °C and PZT/Pt/Ti/TiO_2/SiN_x/Si with TiO_2 deposited at 700 °C having similar PZT thickness. The estimated RMS surface roughnesses were 0.6 nm and 0.9 nm in these platinised PZT/PST/SiO_2 and PZT/TiO_2/SiN_x stacks respectively. The results established that a homogenous film surface with lower roughness can be achieved by inserting PST as a diffusion barrier in the PZT device structures, similar to commonly used barrier TiO_2 layer. It is to be noted that buffer PST layer needs lower crystallisation temperature compared to TiO_2 film. The apparent variation in texture of the PZT film in these two device structures as shown in Fig. 10(a) and (b) can be attributed to the effect of incorporating different types of structural layer in the transducer design, the different deposition techniques and thermal treatment of the barrier layer. These factors are expected to alter the film density, porosity and crystalline phase nucleation, thus having an impact on final PZT microstructures. There are several contributing factors in determining quality of the PZT device structures such as lattice mismatch and thermal expansion mismatch between the buffer PST and the substrates, and strain in the film arising during deposition process [5,22,23]. For example, the lattice parameter (a-axis) of $PS_{60}T$ composition is 0.3919 nm, giving a lattice mismatch only of ~2.9% between PZT (a = 0.4035 nm for 111) and PST, whereas lattice mismatch between Pt (a = 0.3923 nm) and PST is only ~0.11% [5,12]. The useful lattice parameters and thermal expansion coefficients of the materials used in this study are listed in Table 1. It should be noted that the nature of interactions at the film-substrate interface and in multilayer ferroelectric stacks during high temperature annealing and cooling plays crucial role modifying the dielectric properties and the final device structure [24,25]. The internal stresses in ferroelectric thin films and strain-accommodating mechanisms have been thoroughly investigated highlighting the formation of domain patterns and polydomain during the phase transition [24,26] and in particular, revealing the dependence of dielectric tunability of the films on thermal strains upon cooling down through the Curie temperature from higher crystallisation temperature [25]. A systematic analysis of thermal stress in the PST film with variation in Sr content and the nature of stress, e.g. tensile or compressive caused by the thermal treatment including its relation with film microstructures was required to develop an in-depth knowledge of the device properties which is beyond the scope of this paper presented here. In this paper we have presented a qualitative analysis of the PST film as a barrier focussing on the possible integration in PZT transducer stacks and compared the microstructure development of the PZT/PST stacks to other commonly used barrier materials such as TiO_2 films. In particular, the PST film possesses a perovskite-type structure similar to PZT film and gives a lower lattice mismatch to PZT and Pt electrode as illustrated in Table 1. The preliminary results on structural evaluation of the PZT/PST

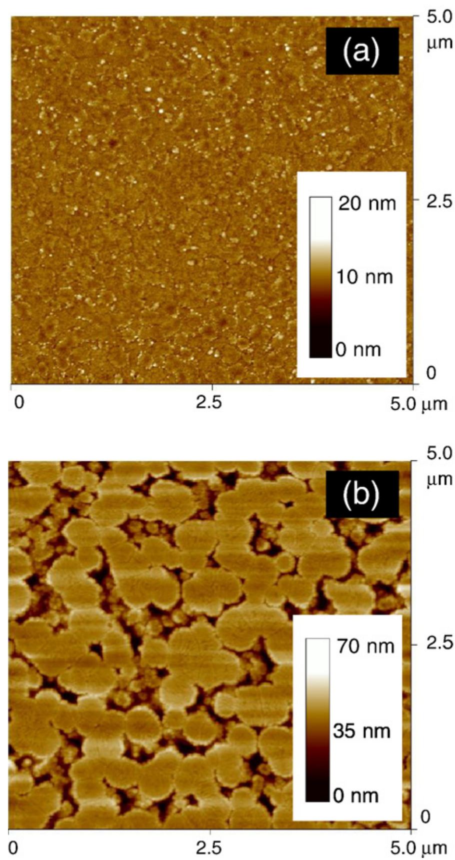

Fig. 9. AFM surface morphology of the PST film on SiO_2/Si substrates at different annealing temperature (a) PST/SiO_2/Si at 600 °C showing RMS roughness of 0.8 nm and (b) 700 °C showing RMS roughness of 7.6 nm.

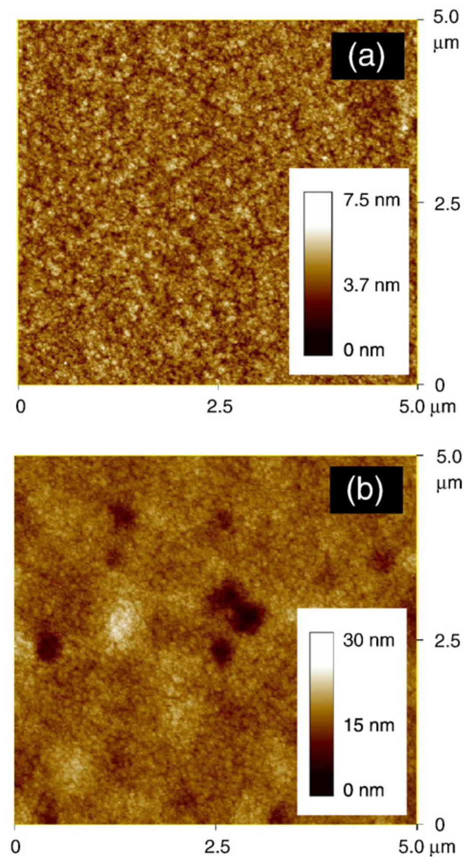

Fig. 10. AFM surface analysis of the PZT films spin-coated on (a) Pt/Ti/PST/SiO_2/Si structure with PST deposited at 550 °C and (b) Pt/Ti/TiO_2/Si_3N_4/Si with TiO_2 deposited at 700 °C.

composites demonstrated that barrier PST layer could provide energetically favourable growth conditions producing sufficient nucleation sites during its crystallisation on Si/SiO_2 substrates under controlled thermal treatment in the temperature range of 550–600 °C. This produces a crack-free smooth crystalline surface of underlying PST film that enhances further the transformation of preferred (111) perovskite phase of the PZT thin film on its top in PZT device structures.

3.3. Electrical characterisation

The electrical characterisation of the PZT device structures inserting a buffer PST layer deposited at 550 °C, e.g. Cr/Au/PZT/Pt/Ti/PST/SiO_2/Si was performed to assess the dielectric properties and polarisation hysteresis of the PZT film. The electrical performance was further analysed by comparing dielectric properties of the PZT having similar thickness of around 0.5 μm deposited on a different template, in this case Cr/Au/PZT/Pt/Ti/TiO_2/SiN_x/Si with TiO_2 as a barrier. Fig. 11 shows the frequency dispersion of the dielectric constant (ε_r) and loss factor (tanδ) obtained from both types of PZT device structures. The frequency range for these measurements was chosen between 1 kHz to 300 kHz applying a weak ac voltage excitation of 100 mV to preserve the polarisation state of the film. The dielectric constants in these PZT device structures having buffer PST and TiO_2 layer were estimated as 415 and 401 at 1 kHz respectively and are quite similar, typically observed in PZT thin film of 30/70 compositions [27]. As the frequency was varied, the dielectric properties in both types of PZT samples exhibited similar nature of the plots with ε_r decreasing gradually with increasing frequency and the loss, tanδ increased. The dielectric constant had a small variation in values of around 5% only, for example higher value of $\varepsilon_r = 390$ at 100 kHz obtained from the PZT stacks with buffer PST compared to $\varepsilon_r = 372$ in PZT sample with TiO_2 barrier as shown in Fig. 11(a) and (b) respectively. The comparison of the dielectric loss measurements with frequency illustrated in Fig. 11 (c) and (d) exhibited slightly higher loss, tanδ in PZT/PST/SiO_2 structures compared to PZT/TiO_2/SiN_x stacks. However the dielectric loss was not significant in either type of device structures and was very low only 0.034 and 0.025 at 100 kHz in PZT/PST and PZT/TiO_2 stacks respectively showing similar nature of the dielectric loss in agreement with published results obtained from PZT thin film devices [28,29]. The slight variations in dielectric constants and loss can be attributed to the interface effect produced by the different combinations of buffer and structural layers on PZT including lattice mismatch, thermal expansion mismatch and the contribution of domain structures [24,25,28] as discussed in Sections 3.1 and 3.2. The ferroelectric behaviour of the PZT having underlying PST barrier was assessed by measuring the polarisation hysteresis loop as shown in Fig. 12. The saturation polarisation, remnant polarisation and coercive

Table 1
The lattice constants and thermal expansion coefficients of materials chosen in PZT transducer design (data are approximate).

Materials	Lattice constant (Å)	Thermal expansion coefficient (10^{-6})/K)
PZT	4.035 (a_0-axis)	7.0
PST	3.919 (a_0)	12.0
Pt	3.923 (a_0)	14.2
Ti	2.950 (a_0)	6.5
TiO_2	4.545 (a_0)	8.5
Si_3N_4	–	3.3
SiO_2	–	0.5
Si	5.431	2.6

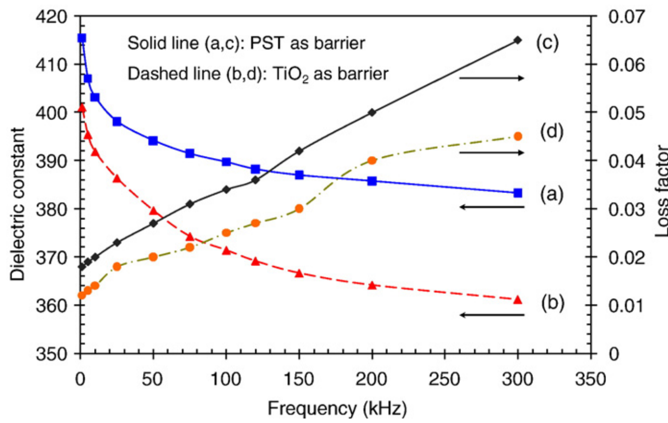

Fig. 11. The frequency dispersion of the dielectric constant and loss factor of PZT thin film deposited on: (a,c) Pt/Ti/PST/SiO_2/Si structure with buffer PST annealed at 550 °C and (b,d) Pt/Ti/TiO_2/Si_3N_4/Si with buffer TiO_2 deposited at 700 °C.

field were 39 μC/cm^2, 28 μC/cm^2 and 104 kV/cm respectively at the maximum applied voltage of 19 V which is consistent with data obtained from PZT film on standard platinised substrates [5,27]. It was further noticed that the hysteresis loop showed asymmetric polarisation states of the PZT having preference towards positively poled state, e.g., unstable negatively poled state as evident from the slight off-set at zero-bias and remnant polarisation values as depicted in Fig. 12. The asymmetric nature of the polarisation states indicates an internal electric field within the PZT device layer that could be induced due to the different top and bottom electrode interfaces leading to the imprint failure as observed in the memory devices [30]. Although the imprint failure has been reported in PZT thin film devices [30], the buffer PST layer is expected to have less effect on such polarisation asymmetry. As the piezoelectric coefficients (d_{31} and d_{33}) are proportional to the remnant polarisation, the large value of the remnant polarisation can be obtained from the PZT/PST structures under optimised design producing stronger piezoelectric effect [29]. The initial characterisation of the PZT/PST device structures established that the PZT film having a buffer PST layer underneath had fully crystallised in the perovskite phase exhibiting similar dielectric and ferroelectric behaviour as observed in the PZT thin films. In this study, we have not measured the piezoelectric coefficients of the PZT film. However, it is envisaged from the preliminary results on dielectric properties and hysteresis loops that the PZT/PST composite with PST diffusion barrier has potential for providing comparable piezoelectric performance as typically observed in PZT device structures having commonly used barrier materials such as TiO_2 layer.

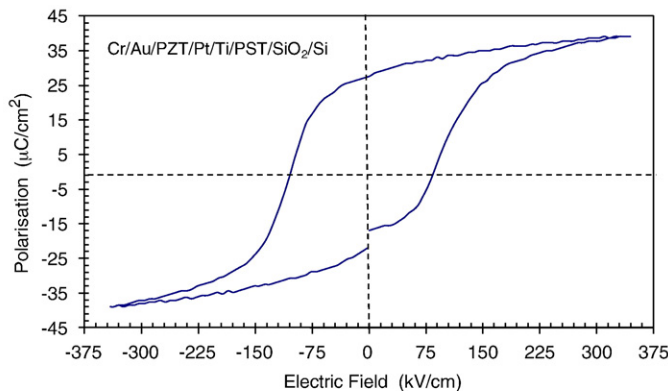

Fig. 12. Polarisation hysteresis loop of the PZT thin film on Pt/Ti/PST/SiO_2/Si stacks inserting buffer PST layer deposited at 550 °C.

4. Conclusions

A sol–gel derived $PbZr_{30}Ti_{70}O_3$ (PZT) device structure was fabricated by incorporating the $Pb_{40}Sr_{60}TiO_3$ thin film as a diffusion barrier between the SiO_2/Si substrate and Pt/Ti bottom electrode. Initial structural evaluation of the PZT thin film on PST/SiO_2/Si template without a bottom Pt/Ti electrode using SEM and AFM methods demonstrated that a crack-free and smooth crystalline surface can be achieved under carefully controlled thermal treatment of buffer PST layer at crystallisation temperature in the range of 550–600 °C following sol–gel deposition of the PST. XRD analysis of PZT/PST/SiO_2/Si stacks revealed polycrystalline nature of the PST and PZT thin films exhibiting random grain orientations, and an insertion of bottom Pt/Ti electrode forming PZT device structure confirmed the perovskite grain transformation producing a preferred PZT (111) phase typically observed in $PbZr_{30}Ti_{70}O_3$ films. The PZT (111) phase showed a gradual decrease in peak intensity along with slight increase of the unfavourable PZT (110) phase with increasing annealing temperature of the buffer PST layer and exhibited a sharp decline in intensity at and beyond 650 °C. XRD patterns of PZT/Pt/Ti/PST/SiO_2/Si stacks were compared to PZT/Pt/Ti/TiO_2/Si_3N_4/Si structures inserting widely used diffusion barrier TiO_2 layer on a different structural layer of Si_3N_4/Si that exhibited similar nature of PZT film orientations in both structures. It was further observed that PST film can be deposited on Si_3N_4/Si and bare Si substrates without any crazing effect and microcracks promoting a preferred PST (110) perovskite phase. The electrical characterisation of Cr/Au/PZT/Pt/Ti/PST/SiO_2/Si device structures with underlying PST barrier deposited at 550 °C exhibited similar range of values for PZT film having dielectric constant and loss factor of 390 and 0.034 at 100 kHz respectively as typically obtained from PZT thin film devices having 30/70 compositions. The ferroelectric behaviour of the PZT film having buffer PST layer underneath was assessed from the measurements of the polarisation hysteresis loops, giving rise to values for the saturation polarisation, remnant polarisation and coercive field of 39 μC/cm^2, 28 μC/cm^2 and 104 kV/cm respectively at an applied voltage of 19 V, which is comparable to data obtained from the PZT transducer stacks on a platinised Si substrate. It is envisaged that the insertion of buffer PST film in PZT transducer design could be advantageous in terms of deposition technique, its relatively low crystallisation temperature and lower cost at wafer-scale production compared to commonly used barrier TiO_2 layer. Initial results have established the potential for PST thin film as a diffusion barrier to deposit high quality PZT thin film on its top and, therefore, PST film could be incorporated in PZT transducer design for future MEMS device applications.

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